REMARKS

Claims 1-4, 6-10, and 12-26 are pending.

Appreciation is expressed for the allowance of claim 15.

Claims 1-4, 6-10, 12-14, and 16-26 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Okuno, U.S. Patent No. 6,105,114 (Okuno) in view of Cliff et al., U.S. Patent No. 6,392,438 (Cliff). These rejections are traversed for at least the reasons set forth below.

Claim 1 was rejected in Section 3 of the Final Office Action. Section 3 states that Okuno fails to teach a storage with a plurality of nonvolatile memory cells.

Section 3 of the Final Office Action states that Cliff discloses a storage with plurality of memory cell array, wherein data could be read or written as a ROM array. In this way Cliff teaches a storage with plurality of nonvolatile memory cells, in order to preserved data from erasure.

Section 3 of the Final Office Action further states that "it would have been obvious to one having ordinary skill in the art at the time of the invention was made to use a nonvolatile memory, wherein nonvolatile memory is able to conserve data even when there is no power supply, as taught by Cliff into [the] system of Okuno in order to preserve data from erasure in case of [a] power shortage. One of ordinary skill in the art would found ample suggestion therein to modify the Okuno system by providing a plurality of nonvolatile memory cells, where each memory cell can preserve one bit of data in event of power failure."

Applicants respectfully submit that claim 1 is allowable over Okuno and Cliff in that one of ordinary skill in the art would not have been motivated to use the circuitry of Cliff configured as a ROM in the memory circuit of Okuno for at least the reasons given below.

Okuno discloses a transposition memory circuit 1 used for performing two-dimensional array transposition of blocks of NxN pixel data to implement a two dimensional discrete cosine

transform (DCT). Okuno, column 1, lines 8-25, column 4, lines 5-9, and column 7, lines 31-47. Circuit 1 of Okuno includes a memory cell array 2 in which data can be written to and read from simultaneously and independent of each other. Okuno, column 10, lines 1-6. Accordingly, when the reading of data (e.g. one pixel) from a cell for a first block of data (of NxN pixel data) is complete, data from a next block of data can be written to the cell. See Okuno, column 9, line 51 to column 10, line 16 where it describes how data from a first block (data that was previously written) is read from the memory cells of array 2 while data from a second block is written to the memory cells of array 2. See also Okuno, column 10, lines 17 to column 10, line 34 where it describes how data from the second block is read from the memory cells of array 2 while data from a third block is written to the memory cells. For accomplishing these operations, memory cell array 2 is responsive to a clock signal for writing data to a memory cell at a rising edge of a clock signal and reading data from a memory cell at a falling edge of a clock signal. Okuno, column 7, lines 48-66.

The ability to perform the operations above enables circuit 1 to perform the transportations of a two dimension array of data with one memory cell array and without using two memory cell arrays. Okuno column 4, lines 32-40; column 5, lines 5-12; column 5, lines 40-42; column 6, lines 6-9 and lines 50-52; and column 11, lines 27-35. The ability to perform these operations without two memory arrays is enabled by the use of a memory array having memory cells that can be written to and read from simultaneously. See Okuno, Column 5, lines 25-27 and lines 44-46; column 6, lines 10-14 and lines 51-54; column 8, lines 37-40; and column 10, lines 1-6. The ability of circuit 1 of Okuno to perform the desired operations without two memory arrays results in reducing circuit scale and power consumption. Okuno, column 4, lines 38-40; column 5, lines 12-14; column 6, lines 21-23 and lines 56-58; and column 11, lines

31-36. Also, such a memory array enables the circuit to have the same processing speed as conventional circuitry. See Okuno, column 5, lines 47-49; column 6, lines 14-15 and lines 24-26, and column 6, lines 54-56.

Cliff teaches a programmable logic array integrated circuit device. See Abstract of Cliff. Cliff teaches that its circuitry can be programmed to implement logic devices such as AND, NAND, OR, or NOR circuits (Column 7, line 27) and can be programmed to perform adder and counter functions (Column 5, lines 63-64).

Section 3 of the Final Office Action states with regard to Cliff that "data could be read or written as a ROM array."

One of ordinary skill in the art would not be motivated to replace memory circuit 2 of Okuno with a ROM array as stated as taught in Cliff in that the circuit of Okuno could not perform its stated purpose (a transposition memory circuit 1 used for performing two-dimensional array transposition of blocks of NxN pixel data to implement a two dimensional discrete cosine transform (DCT)) utilizing a ROM (read only memory) in place of memory circuit 2 of Okuno. As stated above Okuno requires that for memory circuit 2, data can be written to and read from simultaneously and independent of each other during the operation of the circuit.

If the programmable logic array of Cliff is programmed as a ROM (read only memory), then data can not be written to that ROM. See for example, Column 17, lines 8-10 of Cliff where it states that if the RAM regions act like a ROM, "the read-write control signal is held permanently high to force the memory into read mode only." Accordingly, if the circuit of Cliff is programmed as a ROM and implemented into Okuno, then Okuno could not perform its stated purpose because the read-write control signal would be permanently high, preventing data from

being written into the ROM. Thus, without the ability to write data into its memory, the circuitry of Okuno can not perform the function of transposition of blocks of NxN pixel data to implement a two dimensional discrete cosine transform (DCT).

Accordingly, one of skill in the art could not implement circuit 1 of Okuno with the circuit of Cliff programmed as a ROM in that memory circuit 1 of Okuno modified to include a ROM in place of memory circuit 2 could not perform the transposition operations as set forth in Okuno. See MPEP Section 2143.01, Subsection THE PROPOSED MODIFICATION CANNOT RENDER THE PRIOR ART UNSATISFACTORY FOR ITS INTENDED PURPOSE and the subsection entitled THE PROPOSED MODIFICATION CANNOT CHANGE THE PRINCIPLE OF OPERATION OF A REFERENCE.

Section 3 of the Final Office Action states that one of skill in the art would have been motivated to use the memory taught by Cliff in the system of Okuno in order to preserve data from erasure in case of a power shortage. Applicants respectfully submit that this reason would not motivate one of skill in the art to combine the circuit of Cliff programmed as a ROM in the system of Okuno.

First, Okuno teaches a transposition circuit for implementing a transforming coding technique using a two-dimensional discrete cosine transform for coding image data such as MPEG data. Okuno, column 1, lines 8-25. Okuno implements a transposition memory circuit 1 for performing these operations. Okuno, column 7, lines 31-47. The circuit of Okuno is used for decoding multiple blocks of image data with a read and write operation being performed to each cell of array 2 for each block of data being processed. Okuno, column 7, line 31- column 8, line 36.

Nowhere in Okuno does it require circuit 1 of Okuno to be able to store data when the power is off, nor is there any suggestion of it being desirable to save the data in memory array 2. In fact, memory array 2 is not utilized to store data for any substantial period of time. Okuno appears to teach that data is only "stored" in memory array 2 during a cycling of the addresses as provided by counter 20 to perform the transposition operations. See Okuno, column 8, lines 9-13 and in general column 9, line 31 – column 10, line 34. Since circuit 1 is part of a coding system for image data, there is no need to store data in array 2 when circuit 1 does not have power in that circuit 1 would not be used to encode data when there is no power. Because there is no need to store data in array 2 of Okuno (other than for a short period of time during a transposition operation), there is no reason for one of skill in the art to modify Okuno to include the circuit of Cliff programmed to be a ROM for the purpose of saving data during a power outage.

Accordingly, because 1) Okuno teaches that its systems uses an array in which data can be written to and read from simultaneously and independently of each other, and the circuit of Cliff programmed to be ROM can not meet this requirement and 2) because the ability to save the data in memory array 2 of Okuno during a power outage is not a requirement or even desirable, one of skill in the art would not be motivated to modify the circuit of Okuno with the logic array of Cliff programmed as a ROM. Accordingly, amended claim 1 is allowable over Okuno and Cliff.

Claim 6 recites "the array of storage elements comprises a plurality of nonvolatile memory cells," and therefore is allowable over Okuno and Cliff for at least for reasons similar to those given above with respect to amended claim 1.

Pending claim 14 recites "an array of nonvolatile memory cells." Accordingly, amended claim 14 is allowable over Okuno and Cliff for at least reasons similar to those given above with respect to amended claim 1.

Pending claim 16 cites "wherein the array of addressable storage elements comprises a plurality of nonvolatile memory cells." Accordingly, claim 16 is allowable over Okuno and Cliff for at least the reasons similar to those given above with respect to amended claim 1.

Pending claims 22 and 25 each recite "an array of nonvolatile memory cells." Accordingly, pending claims 22 and 25 are allowable over Okuno and Cliff for at least reasons similar to those given above with respect to amended claim 1.

Each dependent claim depends from an independent claim and is allowable for at least this reason.

The application is believed to be in condition for allowance and notice of such is respectfully requested. If there is any remaining issues, the Examiner is respectfully requested to telephone the undersigned.

If Applicant has overlooked any additional fees, or if any overpayment has been made, the Commissioner is hereby authorized to credit or debit Deposit Account 503079

Respectfully submitted,

By: _____

David G. Dolezal
Attorney of Record
Reg. No.: 41,711
Telephone: (512) 996-6839
Fax No.: (512) 996-6854

SEND CORRESPONDENCE TO:

Freescale Semiconductor, Inc.
Law Department

Customer Number: 23125